DIGITAL VIDEO PROCESSING

This invention relates to digital video processing and in one aspect to the processing of a digital video signal with the aim of inhibiting unauthorised copying.

An important example of such a digital video signals is the digital output from devices for playing pre-recorded digital video media such as Digital Versatile Disks (DVD). Suppliers of video programme material are concerned to avoid the creation of unauthorised "pirate" copies by connecting the output of a DVD player to a recorder. There are known methods of modifying an analogue video signal to make it unsuitable for recording without affecting the ability of a display device to show the picture; an example is the "Macrovision" system. However, the advent of digital technology has made it possible to create copies which are undistorted replicas of the original programme. For this reason, suppliers of digital consumer equipment are reluctant to provide any digital output, for the fear that they will be recorded by unauthorised persons.

For as long as display devices operate with analogue inputs, the loss of quality in requiring a digital video signal to be converted to analogue, before it is output from a DVD or other player, could be accepted. There are now, however, digital display technologies which are beginning to be available for consumer use and the lack of availability of digital output signals is becoming a burden.

Professional video equipment almost invariably uses the digital interfaces defined by the ITU/R in their Recommendation 656. These interfaces handle uncompressed digital component (i.e. luminance and colour difference) signals in a universally accepted manner. Integrated circuits which support the bit-serial version of Rec. 656 are readily available. There are thus many advantages to the use of Rec. 656 interfaces in consumer equipment; however, such use has hitherto been discounted because of the concerns relating to the provision of recordable digital outputs.

It is an object of one aspect of the present invention to enable digital video

signals to be output with less concern about unauthorised reproduction.

It is a further object of one aspect of this invention to enable digital video signals in professional formats, such as Rec 656, to be output in a processed or scrambled form which is incapable of being recorded on standard professional equipment.

Accordingly, the present invention consists, in one aspect, in a digital video signal processor having an input adapted to receive a digital video signal having first timing signal references at fixed locations within the line and picture structure; a timing reference stripper for removing said first timing signal references from the digital video signal and a timing reference processor for inserting second timing references into the video signal at locations other than said first locations.

The inventor has appreciated that the parallel and serial digital component interfaces defined in ITU/R Recommendation 656 can be modified to prevent unauthorised use of the digital signal by sending the timing reference signals (TRSs) infrequently, typically once per frame, or by omitting some or all of the blanking and field phase information from the TRSs. Suitably the TRS can be placed other than at the start or finish of a digital active line.

In a further aspect of the invention the transmitted TRSs include additional information about the video, such as its line standard or aspect ratio, or data to confirm the validity of the signal.

Advantageously the order of the bits in the digital words is rearranged, either in a fixed pattern or in a changing pattern synchronised by the transmitted timing reference signals.

In yet another aspect the video data can be modified by subjecting each data word to a scrambling process which substitutes alternative data words for input data words in a manner known only to authorised recipients of the video, and in the event that this process gives words which are only permitted in timing reference signals, re-submits the output words to the scrambling process

repeatedly until a valid word is obtained for transmission

In a simplification of this latter technique, which is applicable where the scrambling process performs modulo-two addition of each bit to an equivalent bit in a "key" word, those output words which are not permitted are replaced by the corresponding unscrambled video words.

In a normal digital component signal in accordance with ITU/R Rec. 656 the TRS's are sent twice per line, and they enable a receiving device, such as a recorder, to identify the order of the words in the multiplex of luminance and colour difference words, and, in the case of the bit-serial interface, they enable the boundaries of the data words to be identified. As well as marking the start and finish of each line, the TRS's identify the start and end of each field and frame.

Existing digital equipment relies for its proper operation on the presence of TRS's at the start and finish of each digital active line and will fail to operate if they are absent. However, if the line standard of the signal is known, the timing reference signals can be regenerated from the data clock, if the position within the frame of one clock pulse is known. Provided a continuous clock signal is present, a single start- or end-of-field TRS enables all the information normally carried by the regular TRS's to be regenerated.

An example of the invention will now be described with reference to the drawings in which:

Figure 1 shows a block diagram of a video scrambling device according to one example of the present invention;

Figure 2 shows the block diagram of a corresponding unscrambling device;

Figure 3 shows a system for scrambling data without introducing certain

code words into the scrambled data; and

Figure 4 shows a simplification of the system of Figure 3.

Referring to Figure 1, a digital video source (1) outputs a parallel (8 bits and clock) signal having the format defined in ITU/R Rec. 656. This signal feeds a digital sync separator (2) and a TRS remover (3). The separator recognises the TRS's in the input signal and decodes the following signals from them: digital line blanking (H), digital field blanking (V) and field phase (F). The TRS remover replaces the TRS's by data corresponding to blanking levels.

The video data without TRS's goes to a modified TRS inserter (4) which inserts a modified TRS once per frame at a fixed point in the video blanking. The modified TRS consists of four data words followed by a further four validation words as follows (in hexadecimal notation):

FF 00 00 IJ $V_{11}V_{12}$ $V_{21}V_{22}$ $V_{31}V_{32}$ $V_{41}V_{42}$

The first three words (FF 00 00) are the same as the first three words of the TRS specified in Rec. 656. The fourth word (IJ) replaces the XY word. It will be understood that the XY word of the TRS specified in Rec. 656 contains information (F) concerning whether the field is odd or even, information (V) concerning vertical blanking, and information (H) concerning horizontal blanking. It follows that the TRS's in a single field of Rec 656 video take a variety of forms and that the TRS's in one field are different from those in the next. The IJ word has its four most significant bits as shown in the table below and the four least significant bits are error detection bits defined in the same way as in the XY word of the TRS described in Rec. 656.

Bit	Value
7	**1**
6	**0**
5	**0** for 16:9 aspect ratio **1** for 4:3 aspect ratio
4	**1** for 625 lines **0** for 525 lines

The validation words ($V_{11}V_{12}$ $V_{21}V_{22}$ $V_{31}V_{32}$ $V_{41}V_{42}$) are fixed and can be used to carry ancillary information such as the method of scrambling or the source of the scrambled signal.

The output of the inserter drives a bit-order rearranger (5) which changes the order of the bits in the word in a changing pattern synchronised by the field phase signal. The resulting signal can be output directly as a scrambled parallel signal (6), or passed to a standard Rec. 656 serialiser (7), which converts the parallel data into a bit-serial stream exactly as described in Rec. 656, to provide a scrambled serial signal (8).

Figure 2 shows an unscrambling device. A scrambled serial digital signal (8) is fed to a standard Rec. 656 deserialiser (21) to provide a parallel data and clock signal to a bit-order rearranger (22). Alternatively, if a parallel scrambled signal (6) is already available, it can be fed directly to the rearranger (22).

The output of the rearranger feeds a TRS detector and decoder (24). The TRS is detected in the conventional manner from its FF and OO words, which are unaffected by the bit reordering.

The TRS detector outputs a synchronising pulse (23) when a valid TRS is detected. The line standard and aspect ratio are also decoded from the relevant bits of the TRS.

The synchronising pulse synchronises a sync pulse generator (25), which is set to the appropriate line standard by the decoded line standard information and driven from the word-rate clock to generate F, V and H signals which are correctly timed to the video data. The location of the TSR in one of the two fields of the frame is used to infer the identification of odd and even fields.

The bit-order rearranger (22) restores the correct order of the bits by the reverse of the process (5) in the scrambling device. The changing pattern of bit-order changes is synchronised by the synchronising pulse (23), which occurs at a fixed position relative to the start of each frame. The resulting parallel digital video signal drives a TRS inserter (26) which inserts standard Rec. 656 TRS's in response to the F, V and H signals from the sync pulse generator (25). The resulting unscrambled parallel signal can be used directly at (27), or serialised in accordance with Rec. 656 in serialiser (28). It should be noted that the TRS insertion is only necessary if a "standard" signal is required for subsequent processing. In most applications, only the output video data from the TRS detector (24) and the F, V and H signals from the sync pulse generator (25) will be required.

It will be recognised that in this example, the TRS's which are inserted to replace the TRS's described in Rec. 656 have the feature that the TRS's are generally identical. This is in contrast to the TRS's described in Rec. 656, where there are different TRS's for start and end of lines, for start and end of fields and for odd and even fields.

Although the above methods give a reasonable level of security, they may not be adequate for all applications and it may be preferable to use a scrambling process for the video data which replaces each video word by another word in a manner known only to intended recipients of the signal. Many such scrambling processes are of course known. However, indiscriminate use of known scrambling processes may convert video words into words which are reserved for synchronisation purposes in the ITU/R or other digital video specification.

Examples are the already mentioned words $FF_{hexadecimal}$ and $00_{hexadecimal}$ which are forbidden in eight-bit systems.

The present invention recognises that it is possible to use any scrambling process, provided that it scrambles the data one word at a time, and has a one-to-one relationship between scrambled words and corresponding input words. (Note that this relationship may change with time in a manner known to authorised recipients of the data, but it must remain constant whilst each word is scrambled.)

In accordance with this invention,It is arranged that when the scrambling process generates an output word which it is not permitted to transmit, an alternative word is sent which will not be mistaken for part of a TRS. The criterion for choosing the replacement word is that it must not correspond to any other word obtained by scrambling legal video data, and thus the unscrambling device will be able to determine that the substitution has taken place.

An example of such a system is shown in Figure 3; the processing shown in this Figure may be interposed between the blocks (3) and (4) in Figure 1.

A video data stream containing no "illegal" words (31) is routed via a changeover switch (32) to a scrambling device (33). The scrambled words are fed to an "illegal" word detection device (34). When an "illegal" word is detected in the scrambled output, a control signal (35) causes the switch (32) to route the output of a temporary storage register (36) to the input of the scrambling device (33). The register (36) holds the output from the scrambling device so that the "illegal" output word is submitted to a second scrambling process in the block (33). If the resulting scrambled word is also "illegal" the process is repeated until a "legal" output word is obtained.

The blocks (32), (33), (34) and (36) all operate at a clock rate higher than that of the video data so that a legal word is present at the output terminal (37) before it is required by the subsequent processing.

The system shown in Figure 3 can be used as an unscrambling system if the block (33) is replaced by an unscrambling device. If the unscrambling process results in an illegal word the process is repeated until a legal output is obtained. This process may be interposed between the blocks (24) and (26) in Figure 2

The maximum number of times that the scrambling or unscrambling process may need to repeat so as to obtain a "legal" output can be shown to be equal to the number of "illegal" words which exist in the set of possible words. For an eight-bit system in Rec. 656, there are two words (out of 256) and for the ten-bit system there are eight "illegal" words (out of 1024).

Here is an example: Suppose that an eight bit video word PQ is to be scambled in a system where the words OO and FF are illegal.

PQ scrambles as 00
00 scrambles as FF
FF scrambles as RS

RS unscrambles as FF
FF unscrambles as 00
00 unscrambles as PQ

A convenient, known scrambling method is to generate a "key" word for each word to be scrambled (in a manner known only to those permitted to unscramble the data), to carry out modulo-two addition of each bit of the key to the corresponding bit of the data, and send the result. This method has the property that, if an output word from it is re-submitted as an input, the resulting "twice processed" output is identical to the original input. In other words, the scrambling process is exactly the same as the unscrambling process. An illustrative example is shown below:.

SCRAMBLING

Input word	0 1 0 0 1 1 0 1
Key word	0 1 1 0 0 1 1 0
Bit-wise modulo-two sum	0 0 1 0 1 0 1 1

UNSCRAMBLING

Input word	0 0 1 0 1 0 1 1
Key word	0 1 1 0 0 1 1 0
Bit-wise modulo-two sum	0 1 0 0 1 1 0 1

This property can be exploited to simplify the system shown in Figure 3 as shown in Figure 4. This shows a process for either scrambling or unscrambling data which may either be interposed between the blocks (3) and (4) of Figure 1, or between the blocks (24) and (26) of Figure 2.

Input data words (51) are fed to a bit-wise, modulo-two adder (52) whose second input is provided with key words from a key generator (53). The result of the addition drives a changeover switch (54) and an illegal word detector (55). Normally, the switch routes the output of the adder to the output terminal (56); however if an illegal word appears at the output of the adder, a control signal (57) causes the switch (54) to route the input data word to the output (56). The illegal word detector (55) and the switch (54) must operate sufficiently fast for the correct data to be present at the switch output before it is required by the subsequent processing.

The above description has been based on eight-bit processing but the skilled man will appreciate that Rec. 656 explains how ten-bit signals are carried by the serial and parallel interfaces and that these methods are directly applicable to the subject matter of the invention. It will also be recognised that other specifications exist for digital video, especially SMPTE 274M and SMPTE 292M for parallel and digital high definition video signals, respectively. The present invention applies in an analogous manner to such other specifications.

It must be recognised that the invention has been described only by way of example and many variations are possible within the concepts described. For example the contents and frequency of transmission of the TRS's could differ from that described here. If the available input is an analogue video signal, or for some other reason lacks the full Rec 656 timing reference signals, the step of stripping those signals is unneccesary and an output component according to this invention will simply insert the new non-standard references.